REMARKS

Preliminarily, Applicant thanks the Examiner for the courtesies extended to Applicant's representative during the telephone interview. The substance of the interview is reflected in the remarks below.

Claims 1-5, 9-16, 20-26, 29-32 and 34-35 remain rejected under 35 § U.S.C. 102(b) over Hobbs (US Patent No. 5,197,138), and claims 6-8, 17-19, 27-28, 33 and 36 remain rejected under 35 U.S.C. § 103(a) over Hobbs in view of Radhakrishna (U.S. Patent No. 6,823,414).

While not conceding the validity of the rejection, but merely to advance prosecution, Applicant has canceled claim 24.

Regarding the remaining claims, Hobbs does not suggest "processing a requested interrupt only when [the/an] interrupt priority value of the requested interrupt is higher than the interrupt threshold value" as explicitly recited in claims 1 and 29, a "common threshold interrupt value," as recited in amended claim 23, or accepting "interrupts having an interrupt priority higher than the interrupt threshold value," as recited in claim 25. The portion of Hobbs to which the Examiner refers merely teaches that "an interrupt will not be recognized or serviced by the processor until the priority of the code thread is lower than the priority of the interrupt." (Emphasis added). See Hobbs column 2, lines 54-57.

Further, comparing two different processor function priorities (i.e., code thread and priority), which vary, as discussed in Hobbs, is different from determining whether a priority of an interrupt is higher than a threshold value, which is fixed, as is claimed. The benefits of this threshold value are explained in paragraph 0027 of the present published application, where it discusses that the fixed threshold value provides global

Docket No.: J0658.0014

Rrutman

Application No. 10/712,473 Amendment dated October 25, 2006

After Final Office Action of July 25, 2006

interrupt handling methodology including an interrupt threshold value (ITV) that effectively represents a global interrupt priority value for all active threads; since any interrupt accepted by thread execution logic must have a higher interrupt priority value than this global interrupt priority value, any interrupt being serviced will always have a higher interrupt priority than any of the active threads, thereby preventing priority

inversion. Therefore, claims 1, 25 and 29, along with their dependent claims, are

patentable over Hobbs.

In view of the above, Applicant believes the pending application is in condition for allowance.

Dated: October 25, 2006

Respectfully submitted,

Laura C. Brutman

Registration No.: 38,395

DICKSTEIN SHAPIRO LLP

1177 Avenue of the Americas

41st Floor

New York, New York 10036-2714

(212) 277-6500

Attorney for Applicant

13

DOCSNY.219719.01